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(57) Abstract :

The present invention discloses a hardware compiler simulation device comprising a programmable logic controller (101), a logic interpreter unit (102), memory buffer (103), synchronizer (104), comparator (105), error notifier (106), and debug unit (107). It enables real-time simulation of logic flow from HDL code without full synthesis, allowing dynamic validation, modular debugging, and accurate timing verification. The device provides rapid error detection and visual feedback, significantly improving hardware-software co-design workflows and reducing development cycles.

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